

Design of asynchronous supervisors

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Abstract

One of the main drawbacks while implementing the interaction between a plant and a supervisor, synthesised by the supervisory control theory of Ramadge and Wonham, is the inexact synchronisation. Balemi was the first to consider this problem, and the solutions given in his PhD thesis were in the domain of automata theory. Our goal is to address the issue of inexact synchronisation in a process algebra setting, because we get concepts like modularity and abstraction for free, which are useful to further analyze the synthesised system. In this paper, we propose four methods to check a closed loop system in an asynchronous setting such that it is branching bisimilar to the modified (asynchronous) closed loop system. We modify a given closed loop system by introducing buffers either in the plant models, the supervisor models, or the output channels of both supervisor and plant models, or in the input channels of both supervisor and plant models. A notion of desynchronisable closed loop system is introduced, which is a class of synchronous closed loop systems such that they are branching bisimilar to their corresponding asynchronous versions. Finally we study different case studies in an asynchronous setting and then try to summarise the observations (or conditions) which will be helpful in order to formulate a theory of desynchronisable closed loop systems.

1 Introduction

Supervisory control theory (RW-theory) [10, 11] performs automatic synthesis of a supervisor which controls a plant such that a corresponding requirement (legal behaviour) is achieved. In control theory terminology,

- the model which is to be controlled is known as *plant*,
- the model which specifies the requirement is known as *specification*,
- the model which forces the plant to meet the specification by interacting with it is known as *supervisor*.

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- the interaction between the plant and the supervisor is known as *closed-loop behavior*.

The closed loop behaviour in RW-theory is realized by synchronous parallel composition. Informally, it allows a plant and a supervisor to synchronise on common events while other events can happen independently.

One of the main drawbacks while implementing the interaction between a plant and a supervisor, synthesised by the supervisory control theory of Ramadge and Wonham, is the inexact synchronization [6]. In practical industrial application the interaction between a plant and a supervisor is not synchronous but rather asynchronous. Due to the synchronous parallel composition, the interaction between the plant and the supervisor is strict. By strict we mean that, either plant or supervisor has to wait for the other party while synchronising. To overcome this problem it is important to study asynchronous communication between the plant and the supervisor where communications are delayed in buffers. The choice of buffers depends on the domain of the system to be modeled. For instance, to model delay insensitive circuits, a wire (see [9]) could be chosen as a buffering mechanism, while to model data-flow networks (see [8]) a queue could be used as a buffering mechanism.

Balemi was the first to consider the inexact synchronisation problem, and the solutions given in his PhD thesis [5] were in the domain of automata theory. In [5] an *input-output* interpretation was given between a plant and a supervisor and a special delay operator was introduced to model the delay in communication. Furthermore, to achieve modularity and abstraction in supervisory control theory, the original theory was extended with the concepts of decentralised control and partial observation, respectively. These concepts were also developed in [5].

The disadvantage of a theory to be based on automata theory is that it requires development of some special concepts like decentralised control for modularity in case of RW-theory. If the theory is based on process algebra, these additional concepts can be attained for free. Congruence is one of the key features in process algebra which helps in achieving this modularity in system design. Modularity is a way of designing a complex system by dividing it into different smaller components or subsystems.

Process algebra is one of the ways in which one can formally specify a system behaviour. It contains different constructs such as sequential composition, and parallel composition which are used as a basic building block to specify any desired behaviour. Apart from this, process algebra also provides modularity in system design, and abstraction from behaviour in system analysis. In this paper we show that it is possible to redesign a synchronous closed loop system in an asynchronous setting by performing three case studies. Finally, some conditions are given which will be helpful in formulating the theory of desynchronisable closed loop systems. A synchronous closed loop system is called desynchronisable iff it is branching bisimilar to a corresponding asynchronous closed loop system.

This report is organized as follows. Section 2 introduces the overall background required for this report and consists of three sub-sections with the following description. In subsection 2.1 we introduce the formal language in which different models (like plant, supervisor or requirement) are specified. In subsection 2.2

we define different buffer models in the specification language. In subsection 2.3 we give a brief introduction on RW-theory and discuss the relation and some results from previous literature with respect to our specification language. In section 3 the work-flow for the different case-studies is given. In particular, it explains how different tools can be used to refine synchronous communication into asynchronous communication. Then the subsections 3.1, 3.2, and 3.3 are devoted to explain three different case studies. Finally, in section 4 we discuss the key conditions which were satisfied by the synchronous closed loop systems in the case studies such that they were branching bisimilar to the corresponding asynchronous version.

2 Preliminaries

2.1 Specification language

We consider the TCP process algebra [4] as the suitable formalism which will be used throughout this paper. This choice is motivated by the following two main reasons:

- One of our goals is to develop this theory and implement it in the current χ [3] tool set as an extended functionality. We know that TCP as a language is a subset of χ and is simpler to work upon, as the latter has a constructs to model hybrid systems while the former is used to model discrete event systems only.
- Previous studies [8, 7, 12] of an asynchronous process composed using buffers used failure equivalence. By studying asynchronous system using TCP we want to find out whether it is possible to state results in a equivalence finer than trace or failure equivalence (see [13], for the lattice of process equivalences).

In this paper we use \mathcal{D} and \mathcal{H} to denote finite sets of data elements and channel names, respectively. Then for each channel $h \in \mathcal{H}$ and each $d \in \mathcal{D}$, assume the presence of the following atomic actions:

- $h!d$: send a data element d at channel h ,
- $h?d$: receive d at channel h , and
- $h\diamond d$: communicate d at channel h .

The following notation and definition will be used throughout the paper. The complete set of actions is denoted by \mathcal{A} where $\mathcal{A} = \{h!d, h?d, h\diamond d \mid \forall d \in \mathcal{D} \wedge \forall h \in \mathcal{H}\}$. Then the communication function $\gamma : \mathcal{A} \times \mathcal{A} \rightarrow \mathcal{A}$ is defined for all $h \in \mathcal{H}$ as $\gamma(h!d, h?d) = \gamma(h?d, h!d) = h\diamond d$ and undefined otherwise. Define the blocking set as $\mathcal{B} = \{h?d, h!d \mid d \in \mathcal{D} \wedge h \in \mathcal{H}\}$ and the hiding set as $\mathcal{I} = \{h\diamond d \mid d \in \mathcal{D} \wedge h \in \mathcal{H}\}$. The set of all process terms (denoted by \mathbf{P}) is then defined by the following grammar:

$\mathbf{P} \triangleq$	$\mathbf{0}$	deadlock process
	$\mathbf{1}$	empty process or <i>skip</i>
	$h!d \cdot \mathbf{P}$	action prefix, where $! \in \{?, !, ?\}$
	$\mathbf{P} + \mathbf{P}$	alternative composition
	$\mathbf{P} \parallel \mathbf{P}$	parallel composition
	$\partial_B(\mathbf{P})$	action encapsulation, where $B \subseteq \mathcal{B}$
	$\tau_I(\mathbf{P})$	abstraction (hiding of actions), where $I \subseteq \mathcal{I}$
	$\rho_f(\mathbf{P})$	renaming of process, where $f : \mathcal{A} \rightarrow \mathcal{A}$.
	\mathcal{R}	recursive definition

The notation \mathcal{R} denotes a recursion definition by a set of pairs $\{X_0 = t_0, \dots, X_m = t_m\}$ where X_i denotes a recursion variable and t_i the process term defining it. The formal semantics for these operators can be found in [4].

Note that in the above definition of process terms it is possible that a process may have the same channel for sending and receiving a data element. But such processes causes a problem while constructing an asynchronous closed loop system from its synchronous counter part. The problem is following: "Suppose a process X has $h?a$ and $h!b$ in its alphabet. Then the information whether h is an input or an output channel is unknown. In this paper we construct an asynchronous process by introducing input queues in input channels and output queues in output channels. The difference between input and output queues will be cleared later in Section 3. Thus, the information whether an input or an output queue should be attached with channel h becomes unclear".

In order to simplify things, we assume that every process has different channels for sending and receiving. Let $\alpha(Q)$ denote the alphabet (see [4]) of a process Q . Formally, a process $Q \in \mathbf{P}$ is called a simple process iff $\forall h, d. [h!d \in \alpha(Q) \Rightarrow \exists d'. [h?d' \in \alpha(Q)]]$ and vice versa. We will work with plants and supervisors which are specified as simple processes.

We now introduce the transition system for a process and for a synchronous closed loop system which will be helpful in defining conditions, presented in Section 4. A transition system generated by a process $X \in \mathbf{P}$ is denoted by quintuple $T_X = (Q_X, \rightarrow_X, q_X^i, A_X)$, where Q_X denotes the set of states, $\rightarrow_X \subseteq Q_X \times A_X \times Q_X$ is the transition relation, q_X^i is the initial state of the process X , and $A_X \subseteq \mathcal{A}$ is the alphabet of X . In this paper we make distinction between a transition system for a process and a transition system for synchronous (or asynchronous) closed loop system. This distinction is based on the alphabet of a process, i.e. for a process X which can be used to model a plant or a supervisor the alphabet of X should be a set $B \subseteq \mathcal{B}$ while for a closed loop system Y it should be a set $I \subseteq \mathcal{I}$. We use notation T_X for a transition system of a process X , T_{SC} for a synchronous closed loop system. In the next subsection we define the different buffer processes which will be used later to study asynchronous communication with respect to these different kinds of buffer.

2.2 Buffer models

In the previous subsection we defined the syntax of the formal language which will be used for specifying plant, supervisor, requirement and buffers. A buffer is a process which receives data from another process and stores that data until another process reads it. For example, a buffer can be a queue (FIFO), or a

stack (LIFO), or a wire, or a bag. Before defining the different buffer processes in the above language, we need to define an auxiliary set for channels. This is necessary for the conversion of a given synchronous closed system into an asynchronous one. So assume that the set \mathcal{H} is closed under $\hat{\cdot}$, i.e. if $h \in \mathcal{H}$ then also $\hat{h} \in \mathcal{H}$. Then define renaming functions $\hat{f} : \mathcal{H} \rightarrow \mathcal{H}$ and $f : \mathcal{H} \rightarrow \mathcal{H}$ as follows:

- for any $k \in \mathcal{H}$, $\hat{f}(k) = \hat{k}$,
- for any $\hat{k} \in \mathcal{H}$, $f(\hat{k}) = k$,
- for $k \in \mathcal{H}$ not in the image of \hat{f} , $f(k) = k$.

The subscript notation f_i (f_o) is used to indicate the renaming of input (output) channels only. Now we give the formal definition for different types of buffers.

Definition 2.1. (Queue). Let ε denote the empty list. Let ξ denote a list of data elements. Let $e.\xi$, and $\xi.d$ denote a list with first element e and last element d , respectively. Then, a queue with input channel $h \in \mathcal{H}$ and output channel $\hat{h} = f(h)$ is specified as follows:

$$\begin{aligned} \mathcal{Q}_h(\varepsilon) &= \sum_{d \in \mathcal{D}} h?d \cdot \mathcal{Q}_h(d.\varepsilon) \\ \mathcal{Q}_h(\xi.d) &= \hat{h}!d \cdot \mathcal{Q}_h(\xi) + \sum_{e \in \mathcal{D}} h?e \cdot \mathcal{Q}_h(e.\xi.d) \\ &\quad (\text{for every } \xi \in \mathcal{D}^*, d \in \mathcal{D}.) \end{aligned}$$

Now define a queue for every set of channels $H \subseteq \mathcal{H}$:

$$Queue_H = \parallel_{h \in H} \mathcal{Q}_h(\varepsilon) \quad \square$$

Definition 2.2. (Stack). A stack with input channel $h \in \mathcal{H}$ and output channel $\hat{h} = f(h)$ is specified as follows (with parameters as in definition 2.1):

$$\begin{aligned} \mathcal{S}_h(\varepsilon) &= \sum_{d \in \mathcal{D}} h?d \cdot \mathcal{S}_h(d.\varepsilon) \\ \mathcal{S}_h(d.\xi) &= \hat{h}!d \cdot \mathcal{S}_h(\xi) + \sum_{e \in \mathcal{D}} h?e \cdot \mathcal{S}_h(e.d.\xi) \\ &\quad (\text{for every } \xi \in \mathcal{D}^*, d \in \mathcal{D}.) \end{aligned}$$

Now define a stack for every set of channels $H \subseteq \mathcal{H}$:

$$Stack_H = \parallel_{h \in H} \mathcal{S}_h(\varepsilon) \quad \square$$

Definition 2.3. (Wire). A wire with input channel $h \in \mathcal{H}$ and output channel $\hat{h} = f(h)$ is specified as follows (with parameters as in definition 2.1):

$$\begin{aligned} \mathcal{W}_h(\varepsilon) &= \sum_{d \in \mathcal{D}} h?d \cdot \mathcal{W}_h(d.\varepsilon) \\ \mathcal{W}_h(d) &= \hat{h}!d \cdot \mathcal{W}_h(d) + \sum_{e \in \mathcal{D}} h?e \cdot \mathcal{W}_h(e). \end{aligned}$$

Now define a wire for every set of channels $H \subseteq \mathcal{H}$:

$$Wire_H = \parallel_{h \in H} \mathcal{W}_h(\varepsilon) \quad \square$$

Definition 2.4. (Bag). Let \emptyset denote the empty multiset. Let ξ denote a multiset of data elements. Let $\xi \uplus \{e\}$ denote the multiset ξ with the multiplicity of e increased by 1 and $\xi \mathbin{\frown} \{e\}$ denote the multiset ξ with the multiplicity of e decreased by 1. Then, a bag with input channel $h \in \mathcal{H}$ and output channel $\hat{h} = \hat{f}(h)$ is specified as follows:

$$\begin{aligned} \mathcal{B}_h(\emptyset) &= \sum_{d \in \mathcal{D}} h?d \cdot \mathcal{B}_h(\emptyset \uplus \{d\}) \\ \mathcal{B}_h(\xi) &= \sum_{e \in \xi} \hat{h}!e \cdot \mathcal{B}_h(\xi \mathbin{\frown} \{e\}) + \sum_{f \in \mathcal{D}} h?f \cdot \mathcal{B}_h(\xi \uplus \{f\}) \\ &\quad (\text{for every } \xi \in \mathcal{D}^*, d \in \mathcal{D}.) \end{aligned}$$

Now define a bag for every set of channels $H \subseteq \mathcal{H}$:

$$Bag_H = \parallel_{h \in H} \mathcal{B}_h(\emptyset) \quad \square$$

2.3 Supervisory control theory

In this subsection we give a brief introduction to the RW-theory in our setup. The basic building block in RW-theory is a deterministic automaton. Plants and supervisors are allowed to perform actions or events which are divided into two disjoint subsets: controllable events and uncontrollable events, i.e. $\mathcal{D} = \mathcal{D}_c \uplus \mathcal{D}_{uc}$. The idea behind this partition is that the supervisor can enable or disable controllable events so that the closed loop behavior is the same as the specification under language equivalence. Furthermore, it can observe but cannot influence uncontrollable events.

The two basic differences from the original theory and the current setup are following. Firstly, we use processes as the building blocks instead of automata. As a consequence we work with finer equivalence than language equivalence. Secondly, we follow the input-output interpretation [5] between a plant and a supervisor (see Figure 1). In this interpretation the uncontrollable events are outputs from a plant to a supervisor and the controllable events are outputs from a supervisor to a plant.

Next we introduce the term deterministic process which will be helpful in defining a plant, supervisor and requirement models in our setup.

Definition 2.5. A process $Y \in \mathbf{P}$ is called a deterministic process [4] if and only if for all states Y of the transition system (generated by the operational rules) it holds that $Y \xrightarrow{a} U \wedge Y \xrightarrow{a} Z \Rightarrow U \equiv Z$, where $U, Z \in \mathbf{P}$, and $U \equiv Z$ means U and Z are syntactically equivalent.

The three basic entities in the RW-theory are: a plant, a supervisor, and a requirement. A plant is a simple and deterministic process $P \in \mathbf{P}$ that does not contain communication actions. The requirement of determinism is necessary because the RW-theory (and its synthesis tool TCT [15]) is based only on deterministic finite automata. The condition that a plant process does not

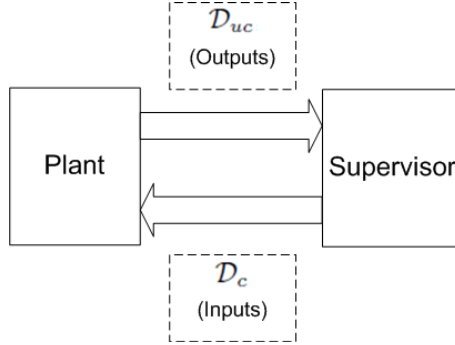


Figure 1: Context diagram for plant and supervisor.

contain communication actions can be stated formally as $\partial_{\mathcal{I}}(P) \Leftrightarrow P$. The requirement of the above condition is due to the construction of asynchronous processes which is explained in detail in following lines. Buffers (like queues, stack, etc) are introduced in both input and output channel. So if communication actions (like $h?d \in I$) are allowed in the specification of a plant process then the information whether the channel h would be an input or an output channel of the plant process is unknown. Similarly, a supervisor is a simple and deterministic process $S \in \mathbf{P}$ such that $\partial_{\mathcal{I}}(S) \Leftrightarrow S$.

A requirement is a process which specifies the legal interaction that should occur while the plant and supervisor are interacting such that a required task (for which supervisor is synthesised) is completed. Thus, a requirement is a deterministic process $E \in \mathbf{P}$ such that $\partial_{\mathcal{B}}(E) \Leftrightarrow E$. This condition suggests that a requirement process should contain only communication actions in its alphabet.

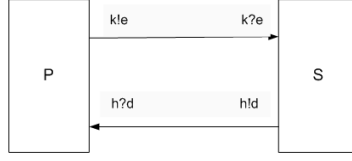
Now we can state the control problem as follows: find a supervisor S for a given plant P and a given requirement E such that,

$$\partial_{\mathcal{B}}(P \parallel S) \Leftrightarrow E.$$

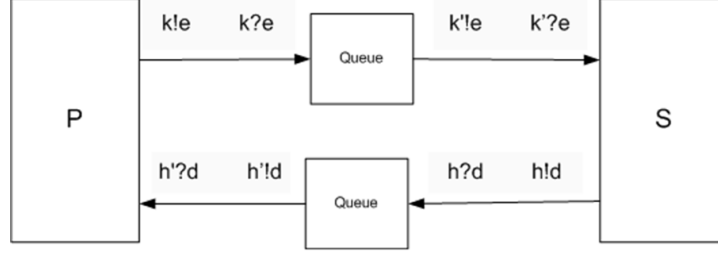
In this paper we do not consider how the supervisor is computed and rather use the solution [15] which provides a closed loop system $\partial_{\mathcal{B}}(P \parallel S)$ strongly bisimilar to a requirement E . Then the aim of this paper is to check whether it is possible to construct an asynchronous closed loop system (Figure 2(b)) such that it is branching bisimilar with its corresponding synchronous closed loop system (Figure 2(a)).

3 Approach

As already discussed in the introduction section, it is important to study an asynchronous interaction between a plant and a supervisor to model an industrial application. So in this section we first give four ways to construct an asynchronous closed loop system from a given synchronous closed loop system. Then, a work-flow is presented which explains how different tools can be used to refine synchronous communication into asynchronous communication in a straightforward and correct way. Later we redesign three case studies in an



(a) Synchronous closed loop system.



(b) Asynchronous closed loop system.

Figure 2: Illustration of the research question.

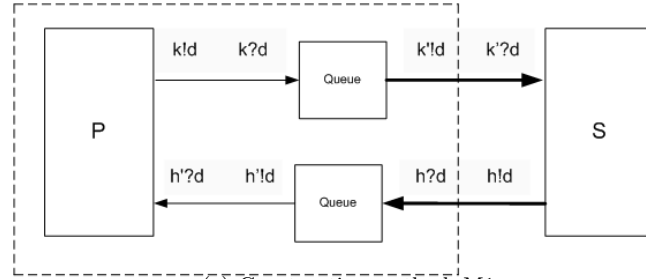
asynchronous setting based upon the above work-flow and methods which were already modelled by the System Engineering group of Eindhoven university of technology (TU/e) in the synchronous setting [14].

A synchronous closed loop system (Figure 2(a)) can be converted into an asynchronous one by introducing queues (see Figure 2(b)) in following ways:

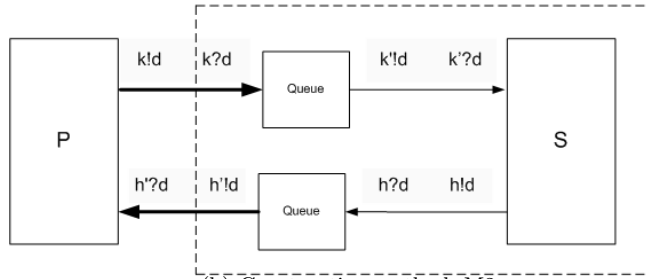
- M1. introducing queues between the plant and supervisor process models such that *the interaction between the plant and queues are hidden* (see Figure 3(a)). The thick lines are used to indicate the visible interaction and thin lines are used to indicate the invisible interaction in Figure 3.
- M2. introducing queues between the plant and the supervisor process models such that *the interaction between the supervisor and queues are hidden* (see Figure 3(b)).
- M3. introducing the queues between a plant and a supervisor such that *the interaction between the output channels of both plant and supervisor with their corresponding queues are hidden* (see Figure 3(c)).
- M4. introducing the queues between a plant and a supervisor such that *the interaction between the input channels of both plant and supervisor with their corresponding queues are hidden* (see Figure 3(d)).

Note that the above indices M1, M2, M3, and M4 are important as they will be used while presenting the results obtained from all the three case studies.

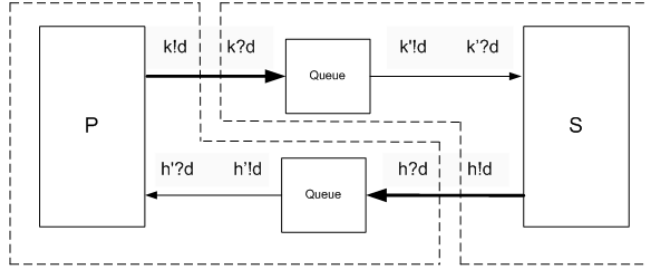
To study an asynchronous interaction between a plant and a supervisor we present the work-flow shown in Figure 4, which checks whether the synchronous and the asynchronous implementation of a plant and a supervisor are equivalent. We check for both branching bisimulation equivalence and weak trace equivalence between the two closed loop systems. Our approach assumes that a plant



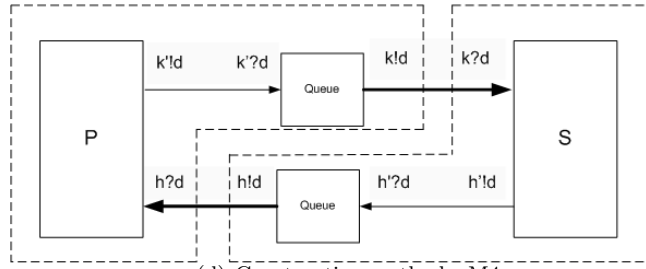
(a) Construction method, M1.



(b) Construction method, M2.



(c) Construction methods, M3.



(d) Construction methods, M4.

Figure 3: Different ways to construct an asynchronous closed loop system.

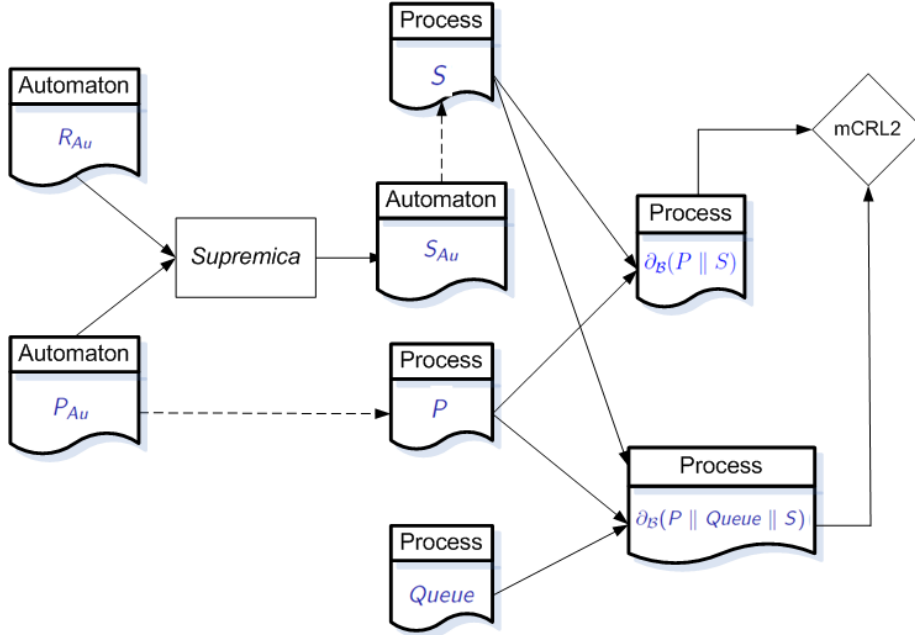


Figure 4: Work-flow for refinement of synchronous communication into asynchronous communication

model and a requirement model are given as automata. The tool *Supremica* [2] is used to synthesise the supervisor for a given plant and a given requirement model. The synthesised automaton is then converted into a process algebraic model in TCP language. Similarly the plant automaton model is also converted into a process algebraic model. This conversion of automaton models into process models is done manually, indicated by the dashed lines (Figure 4). Finally, the tool-set *mCRL2* [1] is used to check for the branching bisimulation relation between a synchronous closed loop and an asynchronous closed loop system designed by each construction method. The following case studies are modified in this report under asynchronous setting:

1. Two machines and a buffer example.
2. Pusher-lift system.
3. Pneumatic cylinder.

For each of the case studies we follow the work-flow as presented. In the next subsections we first introduce the three case studies, and in the last subsection 3.4 we present the overall results obtained in a table. The mCRL2 specification for all the three case studies can be found in Appendix A,B,C.

3.1 Two machines and a buffer example.

This case study is adapted from the examples given in the *Supremica* tool set [2]. The case study consists of two machines which are connected through a buffer.

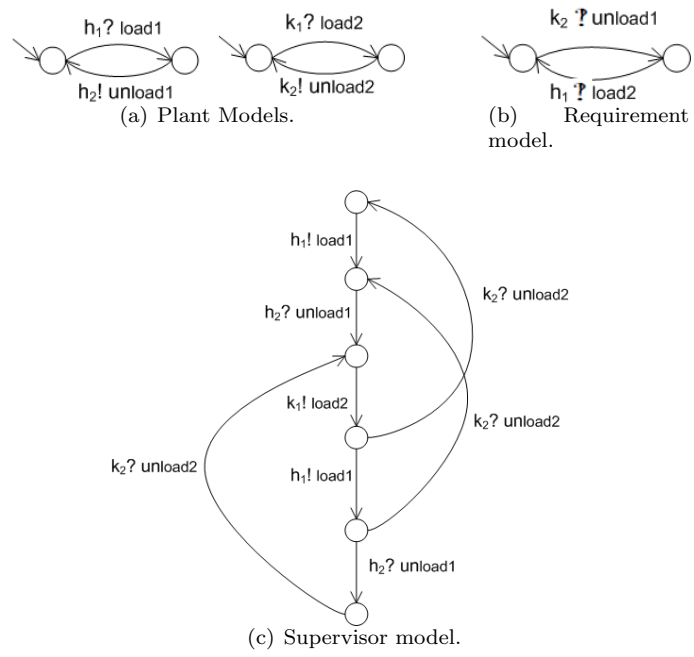


Figure 5: Two machines and a buffer example.

The control task is to synthesise a supervisor which controls the two machines such that the requirement is met, see Figure 5(b). The plant models are shown in Figure 5(a), the requirement model in Figure 5(b) and the synthesised supervisor in Figure 5(c). Note that the synchronous closed loop system for this case study is isomorphic to the supervisor transition system, except for the naming of the action labels. The action labels in a closed loop system will have $?$ symbol, while in a supervisor process they will be annotated with either $?$ or $!$.

The asynchronous system contained finitely many states and the results pertaining to this case study are shown in Figure 12.

3.2 Pusher-lift system [14]

The pusher lift system is a case study taken from a set of lecture notes on supervisory control course [14]. The overall system consists of a lift that can go up and down, a pusher that can retract and extend, and a product holder (see Figure 6(a)). The plant model of the lift is shown in Figure 6(c), pusher and product holder models in Figure 6(b), and the different requirements are shown in Figure 7. The synthesised supervisor model using the Supremica tool is shown in Figure 8. Note that the synchronous closed loop system for this case study is also isomorphic to the supervisor transition system, except for the naming of the action labels.

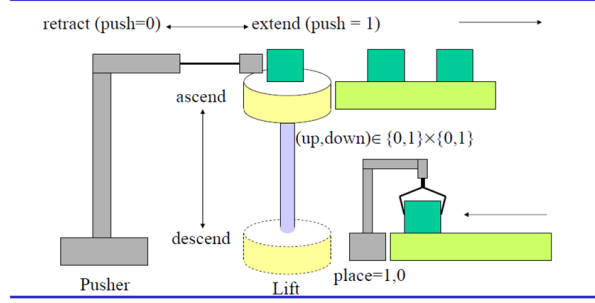
The asynchronous closed loop system composed by all the four construction methods contained a deadlock for this case. Further analyzing the asynchronous closed loop system it was identified that the cause of the deadlock was a self loop in the plant model. This situation is explained by the following example in Figure 9 where a plant, a supervisor and a synchronous closed loop is given.

When the asynchronous closed loop system is designed with the construction method M1, the following trace indicated the deadlock: $\langle h_1?a_1 \cdot h_3?a_3 \cdot h_2?a_2 \cdot \hat{h}_2?a_2 \cdot \hat{h}_1?a_1 \cdot \hat{h}_3?a_3 \rangle$ as the transition $k?b$ is not possible. Note that in the above trace the actions decorated with “ $\hat{}$ ” will be performed by plant model. Moreover, the removal of self loop ($h_2?a_2$) does not affect the synchronous closed loop system and then the above trace will not be valid for the modified asynchronous closed loop.

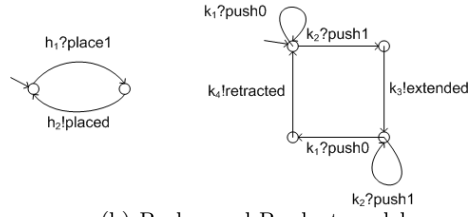
Note that the results obtained for all the construction methods are shown in Figure 12 with respect to both, modified plants (i.e. plant models without self loops) and original plants.

3.3 Pneumatic cylinder [14]

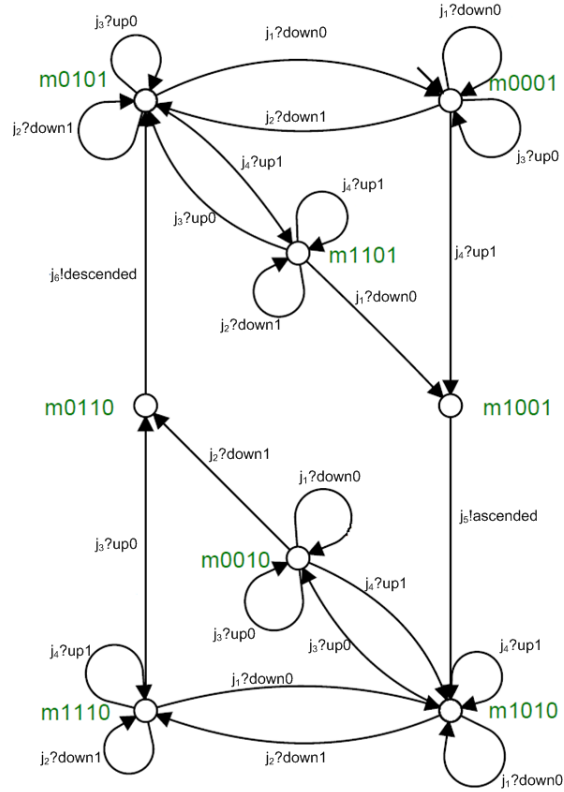
The task in this case study is to design a supervisor that makes a cylinder move out when a push button is activated. Pushing the button will start the extending movement and releasing the button will start the retracting movement (see Figure 10). The control signals ci and co are used to make the cylinder move in and out. The detection of the cylinder being at its innermost (outermost) position is realized through sensor psi (pso). The plant and requirement models are shown in Figure 11(a). The synthesised supervisor is shown in Figure 11(b). Note that the transition system of synchronous closed loop system is again isomorphic to supervisor model, except for the action labelling.



(a) Pusher-lift system [14].



(b) Pusher and Product model



(c) Lift model

Figure 6: Plant models for Pusher-lift system.

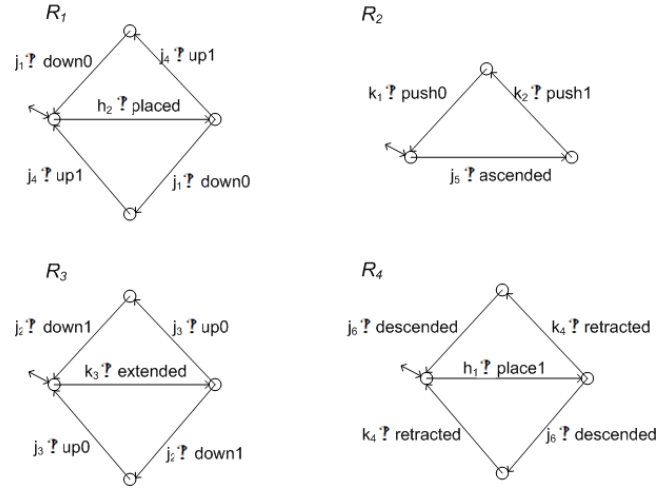


Figure 7: Requirement models for Pusher-lift system.

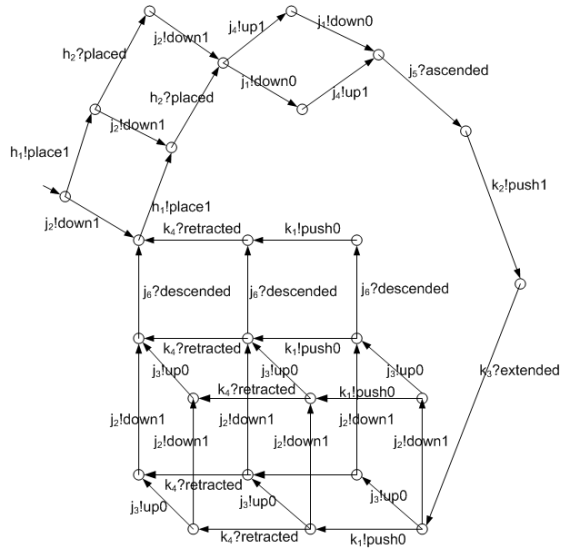


Figure 8: Supervisor model for Pusher-lift system.

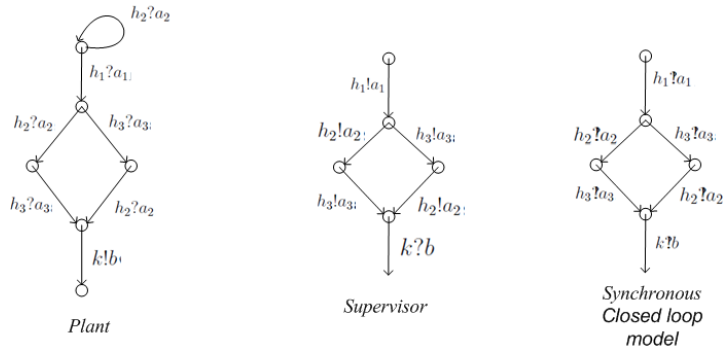


Figure 9: Deadlock caused by the self loop.

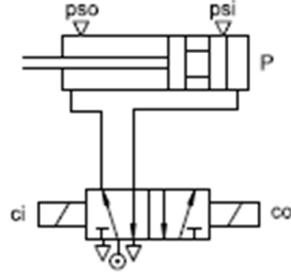
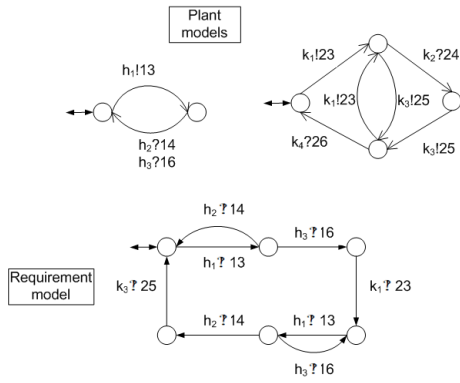
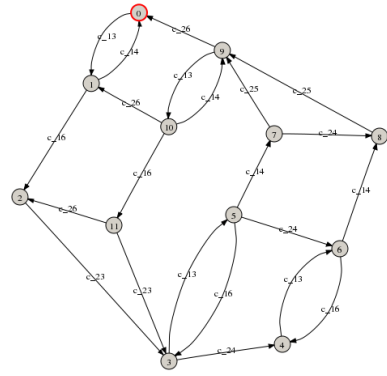


Figure 10: Schematic diagram of pneumatic cylinder [14].



(a) Plant and requirement models for Pneumatic cylinder.



(b) Synchronous closed loop model (Supervisor model) for Pneumatic cylinder.

Figure 11: Pneumatic cylinder case study models.

Results								
	Toy Example		Pusher-lift		Modified Pusher-Lift		Pneumatic cylinder	
Branching bisimilarity	Yes	Yes	No	No	Yes	No	No	No
	Yes	Yes	No	No	No	No	No	No
Weak Trace	Yes	Yes	Yes	No	Yes	No	Yes	No
	Yes	Yes	No	No	No	Yes	No	No

Convention	M1	M2
	M3	M4

Figure 12: Results obtained from all the case studies.

In this case all the asynchronous closed loop systems designed by different methods were containing infinitely many states. To further analyse this system, all the asynchronous closed loop systems were redesigned with 1 place queues. The results pertaining to all the construction methods are shown in Figure 12.

3.4 Results

In this subsection we present the results obtained for all the three case-studies in the Figure 12. The following are the key observations found in the table shown in Figure 12. We use the phrase ‘positive result’ to mean that synchronous closed loop system is equivalent to asynchronous one.

- The construction method M1 yielded positive result for the all case studies with respect to weak trace equivalence.
- In the modified pusher lift case study, only M1 and M3 yielded positive result under weak trace equivalent even though the asynchronous closed loop system constructed by M1 was branching bisimilar to synchronous one.
- The toy example case study had positive results for all the construction methods.

The construction method M1 satisfied the most number of case studies under weak trace and branching bisimulation equivalence. This makes M1 a suitable candidate to further study and answer our research question.

4 Discussion

In this section we sketch the conditions for a synchronous closed loop system to be desynchronisable. A synchronous closed loop system is called desynchro-

nisable iff it is branching bisimilar to the corresponding asynchronous closed loop system. These conditions are important as they prevent the constructed asynchronous closed loop system from deadlocks and generation of infinitely many states. Before we give these conditions formally we need some auxiliary definitions. First, we ask the reader to recall the definitions of transition system of a process, and a synchronous closed loop system as defined in Section 2.1.

Let $\eta : \mathcal{Q}_C \rightarrow 2^{\mathcal{I}}$ be a function which returns a set of enabled actions at a state in a synchronous closed loop system C , i.e. $\eta(q_C) = \{a \mid q_C \xrightarrow{a}\}$, where $q_C \in \mathcal{R}, a \in \mathcal{I}$. Let $\mathbf{Br} : \mathcal{R} \rightarrow \mathbb{N}$ be a function defined as $\mathbf{Br}(q_c) = |\eta(q_c)|$, which is used to access the degree of branching at a state.

Furthermore, we partition the set \mathcal{I} (defined in Section 2.1) into two disjoint subsets $\mathcal{I}_P^i, \mathcal{I}_P^o$ with respect to the given plant process P as:

- $\mathcal{I}_P^i = \{h?a \mid h?a \in \mathcal{I} \wedge h \in \text{inch}(P)\}$.
- $\mathcal{I}_P^o = \{k?a \mid k?a \in \mathcal{I} \wedge k \in \text{outch}(P)\}$.

The following conditions are sufficient for desynchronisability:

1. Plant and supervisor composition must be *well posed*. This term is borrowed from [5] where it was used for similar purpose, i.e. to ensure the asynchronous closed loop system is deadlock free. Consider the transition system $T_P = (Q_P, \rightarrow_P, q_P^i, \mathcal{B})$ for a plant process P . Similarly consider T_S as the transition system of a supervisor process S with $T_S = (Q_S, \rightarrow_S, q_S^i, \mathcal{B})$. Let $N : \mathcal{B}^* \rightarrow \mathcal{B}^*$ be a function defined as: $N(h?a.s) = h!a.N(s)$ and $N(h!a.s) = h?a.N(s)$ for some sequence $s \in \mathcal{B}^*$, and the dot symbol $(.)$ indicates the concatenation of the sequence. Then, the plant and supervisor composition is called *well posed* iff the following conditions are satisfied:

$$\begin{aligned} \forall s \in \mathcal{B}^*, h!a \in \mathcal{A}. [q_P^i \xrightarrow{s}_P q_P \xrightarrow{h!a}_P &\Rightarrow q_S^i \xrightarrow{N(s)}_S q_S \xrightarrow{h?a}_S] \wedge \\ \forall s \in \mathcal{B}^*, h!a \in \mathcal{A}. [q_S^i \xrightarrow{s}_S q_S \xrightarrow{h!a}_S &\Rightarrow q_P^i \xrightarrow{N(s)}_P q_P \xrightarrow{h?a}_P]. \end{aligned}$$

For example, consider a plant process $P = h!a \cdot l?c \cdot P + k!b \cdot \mathbf{0}$ and a supervisor process $S = h?a \cdot l!c \cdot S$. It is easy to verify that the synchronous closed loop system is deadlock free, as $\partial_{\mathcal{B}}(P \parallel S) = h?a \cdot l?c \cdot \partial_{\mathcal{B}}(P \parallel S)$. But when asynchronous closed loop system is designed using construction method M1 it will deadlock, because the plant can reach a deadlock state ($\mathbf{0}$) by performing an action $k!b$.

2. No self loops in either plant model or supervisor model, i.e. both plant and supervisor should not contain a state such that a transition from that state lead into that same state. Let T_P, T_S be the transition system for a plant and a supervisor, respectively. Then, T_j must satisfy the condition $\forall a \in \mathcal{B}, \nexists q_j \in Q_j. [q_j \xrightarrow{a} q_j]$ for $j \in \{P, S\}$.

The need of this condition was explained with an example in Pusher-lift case study (Section 3.2), which resulted in a deadlocked state in asynchronous closed loop system even though the synchronous closed loop system was deadlock free.

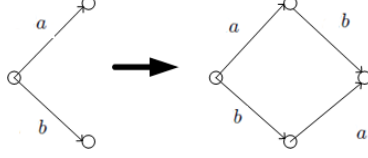


Figure 13: Important property for desynchronisability.

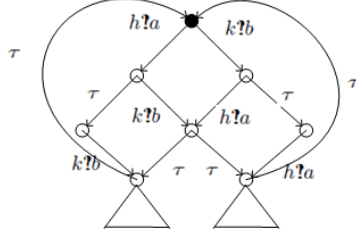


Figure 14: Cycles containing only controllable actions causes infinite states.

3. All the states in a transition system for closed loop system must satisfy the diamond property (see Figure 13). Let T_C be a transition system of a synchronous closed loop system C . Then T_C is said to satisfy diamond property iff the following condition holds

$$\forall a, b \in \mathcal{I}, q, q_1, q_2 \in \mathcal{Q}_C. \left[q \xrightarrow{a} q_1 \wedge q \xrightarrow{b} q_2 \Rightarrow \exists q_3. [q_1 \xrightarrow{b} q_3 \wedge q_2 \xrightarrow{a} q_3] \right].$$

This condition is required for establishing a branching bisimulation relation between a synchronous and an asynchronous closed loop system.

4. All the cycles from the initial state in a synchronous closed loop system must have at least one controllable, and one uncontrollable action in that cyclic trace. Again let T_C be a transition system of a synchronous closed loop system. Then,

$$\forall \pi \in \mathcal{I}^*. \left[q_C^i \xrightarrow{\pi} q_C^i \Rightarrow (\pi \cap \mathcal{I}_P^i \neq \emptyset) \wedge (\pi \cap \mathcal{I}_P^o \neq \emptyset) \right].$$

Note, that we abuse the notation $x \cap A$ to denote the set of elements that occur both in the sequence x and the set A . Intuitively, this condition ensures the progress of the components (i.e. plant and supervisor) in an asynchronous interaction. Consider the following example where $P = (k?b \cdot h?a + h?a \cdot k?b) \cdot P$ and $S = (k!b \cdot h!a + h!a \cdot k!b) \cdot S$. It is clear to see that $\partial_B(P \parallel S) = (k?b \cdot h?a + h?a \cdot k?b) \cdot \partial_B(P \parallel S)$, and there exists a cycle of actions $(h?a \cdot k?b)^*$ such that all actions are controllable actions. In this case the asynchronous closed loop system will have infinite states because supervisor S can always send the controllable actions $k!b$, or $h!a$ to the unbounded queue, and the plant can wait forever to remove these actions from the queue (see Figure 14). In figure 14 the two states with triangles indicate that the transitions from these two states are same as that of the black state. A similar example can also be given in which cycles contain only uncontrollable actions.

Note that the formal proof of the above fact is under construction and will be published in future.

A Final Remark. The transition systems generated by the four methods from a synchronous closed loop system are always isomorphic to each other apart from the difference in abstraction of actions. A hypothesis which one would expect to hold is that, all the four construction methods should always yield an equivalent asynchronous closed loop systems at least modulo weak trace equivalence. But the results shown in the Figure 12 implies that the above hypothesis is not true in general and the abstraction of actions does matter while reducing a transition system (the asynchronous one) even modulo weak trace equivalence. We conclude this report by framing the following open question namely, “which of the construction methods classify a larger class of desynchronisable closed loop system with respect to an equivalence relation?”

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A mCRL2 model for two machine and a buffer example

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Index for action names%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%l1 = load1
%l2 = load2
%ul1= unload1
%ul2= unload2
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

act
s_l1,r_l1,s_l1',r_l1',c_l1,c_l1',s_l2,r_l2,s_l2',r_l2',c_l2,c_l2',
s_ul1,r_ul1,s_ul1',r_ul1',c_ul1,c_ul1',s_ul2,r_ul2,s_ul2',r_ul2',c_ul2,c_ul2';

proc

M1=r_l1'.s_ul1'.M1;
M2=r_l2'.s_ul2'.M2;

%M1=r_l1'.s_ul1.M1;
%M2=r_l2'.s_ul2.M2;

S0=s_l1.S4;
S4=r_ul1.S1;
S1=s_l2.S2;%
S2=r_ul2.S0 + s_l1.S5;

```

```

S5=r_ul2.S4 + r_ul1.S3;
S3=r_ul2.S1;

%S0=s_l1.S4;
%S4=r_ul1'.S1;
%S1=s_l2.S2;
%S2=r_ul2'.S0 + s_l1.S5;
%S5=r_ul2'.S4 + r_ul1'.S3;
%S3=r_ul2'.S1;

Ql1(x1: Int) = (x1==0)-> r_l1.Ql1(x1+1) <>
(s_l1'.Ql1(x1-1) + r_l1.Ql1(x1+1));

Ql2(x2: Int) = (x2==0)-> r_l2.Ql2(x2+1) <>
(s_l2'.Ql2(x2-1) + r_l2.Ql2(x2+1));

Qul1(ux1: Int) = (ux1==0)-> r_ul1'.Qul1(ux1+1) <>
(s_ul1.Qul1(ux1-1) + r_ul1'.Qul1(ux1+1));

Qul2(ux2: Int) = (ux2==0)-> r_ul2'.Qul2(ux2+1) <>
(s_ul2.Qul2(ux2-1) + r_ul2'.Qul2(ux2+1));

Plant=M1||M2;
Supervisor=S0;

init
hide({c_l1',c_l2',c_ul1',c_ul2'},
allow({c_l1,c_l2,c_ul1,c_ul2,c_l1',c_l2',c_ul1',c_ul2'},
comm({s_l1|r_l1->c_l1,s_l2|r_l2->c_l2,s_ul1|r_ul1->c_ul1,
s_ul2|r_ul2->c_ul2,s_l1'|r_l1'->c_l1',s_l2'|r_l2'->c_l2',
s_ul1'|r_ul1'->c_ul1',s_ul2'|r_ul2'->c_ul2'},
Plant||Ql1(0)||Ql2(0)||Qul1(0)||Qul2(0)||Supervisor )))
;

```

B mCRL2 model for Pusher-lift case study.

```

%%%%%%Index for action names%%%%%%%%
%% asc=ascended
%% desc=descended
%% d0=down0
%% d1=down1
%% ext=extended
%% ret=retracted
%% pl1=place1
%% pld=placed
%% pu0=push0
%% pu1=push1
%% up0=up0
%% up1=up1

```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
act
```

```

s_asc,r_asc,s_asc',r_asc',c_asc,c_asc',s_desc,r_desc,s_desc',r_desc',
c_desc,c_desc',s_d0,r_d0,s_d0',r_d0',c_d0,c_d0',s_d1,r_d1,s_d1',r_d1',
c_d1,c_d1',s_ext,r_ext,s_ext',r_ext',c_ext,c_ext',s_pl1,r_pl1,s_pl1',
r_pl1',c_pl1,c_pl1',s_pld,r_pld,s_pld',r_pld',c_pld,c_pld',s_pu0,r_pu0,
s_pu0',r_pu0',c_pu0,c_pu0',s_pu1,r_pu1,s_pu1',r_pu1',c_pu1,c_pu1',s_ret,
r_ret,s_ret',r_ret',c_ret,c_ret',s_up0,r_up0,s_up0',r_up0',c_up0,c_up0',
s_up1,r_up1,s_up1',r_up1',c_up1,c_up1';

```

```
proc
```

```

Pu1=r_pu0'.Pu1+r_pu1'.Pu2;
Pu2=s_ext'.Pu3;
Pu3=r_pu1'.Pu3 + r_pu0'.Pu4;
Pu4=s_ret'.Pu1;

```

```

%L0001=r_d0.L0001+r_up0.L0001+r_up1.L1001+r_d1.L0101;
L0001=r_up1'.L1001+r_d1'.L0101;

```

```
L1001=s_asc'.L1010;
```

```

%L1010=(r_up1+r_d0).L1010 + r_up0.L0010+r_d1.L1110;
L1010=r_up0'.L0010+r_d1'.L1110;

```

```

%L1110=(r_up1+r_d1).L1110 + r_d0.L1010 + r_up0.L0110;
L1110=r_d0'.L1010 + r_up0'.L0110;

```

```

%L0010=(r_up0+r_d0).L0010 + r_up1.L1010 + r_d1.L0110;
L0010=r_up1'.L1010 + r_d1'.L0110;

```

```
L0110=s_desc'.L0101;
```

```

%L0101=(r_up0+r_d1).L0101 + r_d0.L0001 +r_up1.L1101;
L0101=r_d0'.L0001 +r_up1'.L1101;

```

```

%L1101=(r_up1+r_d1).L1101 + r_up0.L0101+r_d0.L1001;
L1101=r_up0'.L0101+r_d0'.L1001;

```

```

Pr1=r_pl1'.Pr2;
Pr2=s_pld'.Pr1;

```

```

%Qpu0(pu0: Int) = (pu0==0)-> r_pu0.Qpu0(pu0+1) <>
% (s_pu0'.Qpu0(pu0-1) + r_pu0.Qpu0(pu0+1));

```

```

%Qpu1(pu1: Int) = (pu1==0)-> r_pu1.Qpu1(pu1+1) <>
% (s_pu1'.Qpu0(pu1-1) + r_pu1.Qpu1(pu1+1));

```

```

S0=s_d1.S11+s_pl1.S22;
S11=s_pl1.S9;

```

```

S22=s_d1.S9 + r_pld.S23;
S9=r_pld.S12;
S23=s_d1.S12;
S12=s_up1.S8 + s_d0.S24;
S8=s_d0.S21;
S24=s_up1.S21;
S21=r_asc.S2;
S2=s_pu1.S4;
S4=r_ext.S6;
S6=s_d1.S18+s_up0.S10+s_pu0.S3;
S18=s_up0.S20 + s_pu0.S15;
S10=s_d1.S20 + s_pu0.S7;
S3=s_d1.S15+s_up0.S7+r_ret.S1;
S20=r_desc.S16+s_pu0.S19;
S15=s_up0.S19+ r_ret.S14;
S7=s_d1.S19+r_ret.S5;
S1=s_d1.S14+s_up0.S5;
S16=s_pu0.S13;
S19=r_desc.S13+r_ret.S17;
S14=s_up0.S17;
S5=s_d1.S17;
S13=r_ret.S11;
S17=r_desc.S11;

Qpu0(x1: Int) = (x1==0)-> r_pu0.Qpu0(x1+1) <>
(s_pu0'.Qpu0(x1-1) + r_pu0.Qpu0(x1+1));

Qpu1(x2: Int) = (x2==0)-> r_pu1.Qpu1(x2+1) <>
(s_pu1'.Qpu1(x2-1) + r_pu1.Qpu1(x2+1));

Qext(x3: Int) = (x3==0)-> r_ext'.Qext(x3+1) <>
(s_ext.Qext(x3-1) + r_ext'.Qext(x3+1));

Qret(x4: Int) = (x4==0)-> r_ret'.Qret(x4+1) <>
(s_ret.Qret(x4-1) + r_ret'.Qret(x4+1));

Qd0(x5: Int) = (x5==0)-> r_d0.Qd0(x5+1) <>
(s_d0'.Qd0(x5-1) + r_d0.Qd0(x5+1));

Qd1(d1: Int) = (d1==0)-> r_d1.Qd1(d1+1) <>
(s_d1'.Qd1(d1-1) + r_d1.Qd1(d1+1));

Qup0(up0: Int) = (up0==0)-> r_up0.Qup0(up0+1) <>
(s_up0'.Qup0(up0-1) + r_up0.Qup0(up0+1));

Qup1(up1: Int) = (up1==0)-> r_up1.Qup1(up1+1) <>
(s_up1'.Qup1(up1-1) + r_up1.Qup1(up1+1));

Qasc(x6: Int) = (x6==0)-> r_asc'.Qasc(x6+1) <>
(s_asc.Qasc(x6-1) + r_asc'.Qasc(x6+1));

```

```

Qdesc(x7: Int) = (x7==0)-> r_desc'.Qdesc(x7+1) <>
(s_desc.Qdesc(x7-1) + r_desc'.Qdesc(x7+1));

Qpl1(pl1: Int) = (pl1==0)-> r_pl1.Qpl1(pl1+1) <>
(s_pl1'.Qpl1(pl1-1) + r_pl1.Qpl1(pl1+1));

Qpld(pld: Int) = (pld==0)-> r_pld'.Qpld(pld+1) <>
(s_pld.Qpld(pld-1) + r_pld'.Qpld(pld+1));

Plant=Pu1||L0001||Pr1;
Supervisor=S0;

init
%%For asynchronous closed loop system.
hide({c_asc',c_desc',c_d0',c_d1',c_ext',c_pl1',c_pld',c_pu0',c_pu1',c_ret',
c_up0',c_up1'}},
allow({c_asc,c_desc,c_d0,c_d1,c_ext,c_pl1,c_pld,c_pu0,c_pu1,c_ret,c_up0,c_up1,
c_asc',c_desc',c_d0',c_d1',c_ext',c_pl1',c_pld',c_pu0',c_pu1',c_ret',
c_up0',c_up1'}},
comm({s_asc|r_asc->c_asc,s_desc|r_desc->c_desc,s_d0|r_d0->c_d0,s_d1|r_d1->c_d1,
s_ext|r_ext->c_ext,s_pl1|r_pl1->c_pl1,s_pld|r_pld->c_pld,
s_pu0|r_pu0->c_pu0,s_pu1|r_pu1->c_pu1,s_ret|r_ret->c_ret,
s_up0|r_up0->c_up0,s_up1|r_up1->c_up1,
s_asc'|r_asc'->c_asc',s_desc'|r_desc'->c_desc',s_d0'|r_d0'->c_d0',
s_d1'|r_d1'->c_d1',s_ext'|r_ext'->c_ext',s_pl1'|r_pl1'->c_pl1',
s_pld'|r_pld'->c_pld',s_pu0'|r_pu0'->c_pu0',s_pu1'|r_pu1'->c_pu1',
s_ret'|r_ret'->c_ret',s_up0'|r_up0'->c_up0',s_up1'|r_up1'->c_up1'}},
(Plant||Supervisor||Qasc(0)||Qdesc(0)||Qd0(0)||Qd1(0)||Qext(0)||Qpl1(0)||
Qpld(0)||Qpu0(0)||Qpu1(0)||Qret(0)||Qup0(0)||Qup1(0))
));

%% For synchrons closed loop system.
%allow({c_asc,c_desc,c_d0,c_d1,c_ext,c_pl1,c_pld,c_pu0,c_pu1,c_ret,c_up0,c_up1},
% comm({s_asc|r_asc->c_asc,s_desc|r_desc->c_desc,s_d0|r_d0->c_d0,s_d1|r_d1->c_d1,
% s_ext|r_ext->c_ext,s_pl1|r_pl1->c_pl1,s_pld|r_pld->c_pld,s_pu0|r_pu0->c_pu0,
% s_pu1|r_pu1->c_pu1,s_ret|r_ret->c_ret,s_up0|r_up0->c_up0,s_up1|r_up1->c_up1}},
%Plant||Supervisor
%));

```

C mCRL2 model for the Pneumatic cylinder

```

act
s_13,r_13,s_13',r_13',c_13,c_13',s_14,r_14,s_14',r_14',c_14,c_14',s_16,r_16,
s_16',r_16',c_16,c_16',s_23,r_23,s_23',r_23',c_23,c_23',s_24,r_24,s_24',
r_24',c_24,c_24',s_25,r_25,s_25',r_25',c_25,c_25',s_26,r_26,s_26',r_26',c_26,c_26';

proc
P0=r_13'.P1;

```



```

P1=(s_14'+s_16').P0;

Q0=r_23'.Q1;
Q1=r_25'.Q3+s_24'.Q2;
Q2=r_25'.Q3;
Q3=s_26'.Q0+r_23'.Q1;

Plant=P0||Q0;

%Note that for this case study 1 place queues are used.
%Because unbounded queues cause infinite states asynchronous
%closed loop system.

Q13(x13: Int) = (x13==0)-> r_13.Q13(x13+1) +
(x13==1)-> (s_13'.Q13(x13-1) + r_13.Q13(x13+1));

Q14(x14: Int) = (x14==0) -> r_14'.Q14(x14+1)+
(x14==1) ->( s_14.Q14(x14-1)+r_14'.Q14(x14+1));

Q16(x16: Int) = (x16==0) -> r_16'.Q16(x16+1) +
(x16==1) -> (s_16.Q16(x16-1)+r_16'.Q16(x16+1));

Q23(x23: Int) = (x23==0)-> r_23.Q23(x23+1) +
(x23==1)->( s_23'.Q23(x23-1)+r_23.Q23(x23+1));

Q25(x25: Int) = (x25==0)-> r_25.Q25(x25+1) +
(x25==1)->( s_25'.Q25(x25-1)+r_25.Q25(x25+1));

Q24(x24: Int) = (x24==0) -> r_24'.Q24(x24+1) +
(x24==1) -> (s_24.Q24(x24-1)+r_24'.Q24(x24+1));

Q26(x26: Int) = (x26==0) -> r_26'.Q26(x26+1) +
(x26==1) ->(s_26.Q26(x26-1)+r_26'.Q26(x26+1));

S0=s_13.S1;
S1=r_14.S0 + r_16.S2;
S2=s_23.S3;
S3=s_13.S4+r_24.S5;
S4=r_16.S3 +r_14.S6+ r_24.S7;
S5=s_13.S7;
S6=r_24.S8+s_25.S9;
S7=r_16.S5+r_14.S8;
S8=s_25.S9;
S9=s_13.S10+r_26.S0;
S10=r_16.S11 + r_26.S1 + r_14.S9;
S11=r_26.S2 + s_23.S3;

Supervisor=S0;
init
%For asynchronous closed loop system

```

```

hide({c_13',c_14',c_16',c_23',c_24',c_25',c_26'},
allow({c_13,c_13',c_14,c_14',c_16,c_16',c_23,c_23',c_24,c_24',c_25,
      c_25',c_26,c_26'},
      comm({s_13|r_13->c_13,s_13'|r_13'->c_13',s_14|r_14->c_14,s_14'|r_14'->c_14',
            s_16|r_16->c_16,s_16'|r_16'->c_16',s_23|r_23->c_23,s_23'|r_23'->c_23',
            s_24|r_24->c_24,s_24'|r_24'->c_24',s_25|r_25->c_25,s_25'|r_25'->c_25',
            s_26|r_26->c_26,s_26'|r_26'->c_26'},
            Plant||Q13(0)||Q14(0)||Q16(0)||Q23(0)||Q24(0)||Q25(0)||Q26(0)||Supervisor
            )))
;
%% For synchronous closed loop sytem
%allow({c_13,c_14,c_16,c_23,c_24,c_25,c_26},
%      comm({s_13|r_13->c_13,s_14|r_14->c_14,s_16|r_16->c_16,
%            s_23|r_23->c_23,s_24|r_24->c_24,s_25|r_25->c_25,
%            s_26|r_26->c_26},
%            Plant||Supervisor
%            ))%
% ;

```